Empower.
Innovate.
Care.

SUMMER PRACTICE 2021

YOUR SUMMER INTERNSHIP IN ONE OF THE FOLLOWING TEAMS:

IC DESIGN & LAYOUT

The IC Design & Layout team is focused on creating the required design and related documentation in order to contribute to the achievement of the projects' targets in terms of product specification, cost, quality and timing.

Main activities in the summer practice:
- Schematic entry of circuit bocks like current mirrors, amplifiers, etc in CMOS technology by means of Cadence Virtuoso Design Suite
- Simulate the blocks with Spectre, taking into account voltage, process and temperature variations
- Make layout of the block with Cadence Virtuoso Layout Suite and perform Design Rule Check (DRC) and Layout vs Schematic (LVS) verifications to ensure the block layout was done properly

PRODUCT VERIFICATION

Product Verification is the process of measurement/determining the fundamental electrical and physical characteristics of new developed (and manufactured) Integrated Circuits.

Main activities in the summer practice:
- Create/develop (or contribute to) specific measurement solution using of benchtop or PXI based instruments (DMM, SMU, Oscilloscope, AWG etc.)
    - Define requirements for measurement setup that best fits IC parameter verification
    - Develop, assemble/wire and debug dedicated hardware setup that meets predefined requirements
- Create (semi)automated test solution (LabVIEW based) that facilitates measurements
- Perform measurements, log data, analyse/interpret results

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INSPIRED ENGINEERING